AMENDMENTS TO THE SPECIFICATION

Please amend the following paragraphs:

[0003] The present invention relates to a method of fabricating a thin film transistor wherein the source and drain regions are formed by doping an active layer with impurities [[by]] using a gate electrode as a mask and ~~by forming a source and a drain~~ by activating the impurities.

[0006] In FIG. 1A, an insulating or buffer layer 13 is formed by depositing an insulating substance, such as silicon dioxide, on a transparent substrate 11, such as a glass substrate or the like, by a [[with]] Chemical Vapor Deposition (hereinafter abbreviated CVD) method. An active layer 15 is formed by depositing polycrystalline silicon on the buffer layer 13 by a [[with]] CVD method and by patterning the polycrystalline silicon by a photolithography process~~. Next, the active layer 15 is patterned by photolithography to be etched on a predetermined portion of the buffer layer 13~~.

[0007] According to FIG. 1B, another layer of silicon dioxide is now grown or deposited across the surface of the silicon wafer. ~~Using similar lithographic techniques to those described above, holes are etched through the silicon dioxide in areas in which it is desired to make the connections and metallization layer of aluminum interconnections are deposited. In other words, after~~ After the silicon dioxide layer covers the active layer 15, a conductive material such as aluminum ~~Aluminum, metal,~~ or the like is deposited on the silicon dioxide layer by a [[the]] CVD process.

[0008] A gate insulating layer 17 and a gate 19 are formed by patterning the conductive material and the silicon dioxide layer by a photolithography process so that they remain over a selected portion of the active layer 15, as shown in FIG. 1B.

[0010] Referring to FIG. 1C, the impurities implanted in the ion-implanted region 21 are activated by application of a laser beam onto the region 21. Consequently, an impurity region 23 constituting source and drain regions ~~a source and a drain~~ is formed as the impurity ions in the region 21 are activated by the laser beam.

[0011] However, [[as]] the above-described method of fabricating a TFT according to the related art ~~reveals, this process~~ involves complicated steps, such as irradiation of the impurity region with a laser beam to form source and drain regions ~~a source and a drain region~~ and activation of the implanted impurity ions.

[0012] The use of laser beams for the activation of the impurity ions is expensive and difficult ~~are costly, not very feasible~~, and can significantly increase the risk of structural damage to the semiconductor layers because of its heat treatment intensity.

[0014] The object of the present invention is to provide a method of fabricating a TFT including the step of simultaneously forming an impurity region for source and drain regions ~~a source and a drain region~~ and the step of implanting and activating the impurity ions in such an impurity region.

[0023] Referring to FIG. 2A, a buffer layer 33 is formed by depositing silicon dioxide or silicon nitride on a transparent substrate 31, such as a glass substrate or the like, by a CVD method ~~using CVD techniques~~. An active layer 35 is formed by depositing undoped polycrystalline silicon on the buffer layer 33 to a thickness between about 400 and 800 Å by a CVD method ~~using CVD techniques~~ or other suitable methods [[technique]] known to one of [[or]] ordinary skill in the art. The active layer 35 is patterned by a photolithography process so that it remains on a predetermined portion of the buffer layer 33.

[0024] Alternatively, rather than forming the active layer 35 by depositing undoped polycrystalline silicon, the active layer 35 may be formed by depositing undoped amorphous silicon by a CVD method ~~using a CVD process~~ and thereafter crystallizing the amorphous silicon with laser annealing or other suitable methods [[process]] known to one of [[or]] ordinary skill in the art.

[0025] As illustrated in FIG. 2B, another layer of an insulating layer, namely, silicon dioxide, is deposited on the buffer layer 33 to cover the active layer 35, and a conductive material, such as aluminum [[Aluminum]] or the like, is deposited on the silicon dioxide by a [[using]] CVD

method. A gate insulating layer 37 and a gate electrode 39 are formed by patterning or etching the conductive material and the silicon dioxide by a photolithography process so that the gate insulating layer 37 and gate electrode 39 are formed over a certain portion of the active layer 35. Preferably, the gate insulating layer 37 and the gate 39 are formed to a thickness of about 500-1500 Å and about 1500-2500 Å, respectively.

[0027] An [[The]] optimal temperature for impurity doping according to the preferred embodiment is ~~a temperature~~ in the range of about 200-300 degrees Celsius. In the preferred embodiment, as the size of the active region 35 increases, the time necessary for the hydrogen ion implantation correspondingly increases in order to achieve the optimal temperature [[range]] between about 200 to 300 degrees Celsius. Therefore, the size of the active region or layer is proportionately related to the hydrogen implantation time required to achieve the optimal ~~an optical~~ temperature.

[0031] The n-type ~~implanted n-typed~~ impurity ions, once implanted into the active layer, become self-activated as the mobility of each ion particle in the excited region 41 increases ~~is increased by the state of excitation of the excited region 41~~. In other words, as the n-type impurity ions are implanted into the excited region 41 ~~is implanted with n-typed impurities~~, they [[it]] simultaneously become [[becomes]] activated, thereby quickly and efficiently forming ~~so as to quickly and efficiently yield~~ a heavily-doped impurity region.

[0033] As explained in the foregoing description, when hydrogen ions are implanted into an active layer, such an implantation process heats the exposed surface of the active layer, thereby forming an excited region. Then, impurity ions are implanted into the excited region, forming a heavily-doped impurity region, as the impurity ions become self-activated in the excited region ~~by self-activation of the implanted impurities~~.

[0034] Accordingly, a method for fabricating a TFT according to the present invention ~~requires no costly activation equipment and~~ does not require an [[the]] additional step of laser annealing, which necessitates an expensive equipment, because [[since]] the impurity region for source and drain regions is formed by a simple, single, and straightforward step of implanting hydrogen ions before implanting impurity ions for the source and drain regions to activate the ~~and~~

~~activating~~ impurity ions simultaneously, which accomplishes both (1) impurity doping; and (2) impurity ion activation.